REMARKS

Disapproval of Drawing Correction

The proposed Drawing correction has been disapproved for allegedly introducing new matter. In response, Applicant submits a new Figure 11. Figure 11 simply sets forth the process of steps of the combination of claims 1 and 4.

Alternatively, Applicant note that in the First Office Action, the Examiner objected to the Drawings and stated that "The Drawings must show every feature of the invention specified in the claims. Therefore, the limitations of claim 4...must be shown..." Claim 4 reads:

> "The process of Claim 1, further comprising testing the connection between the first and second circuit patterns prior to the step of separating the common substrate into separate substrates."

The correction to the drawings was simply to show a testing apparatus labeled 60 in Figure 5 in a state of testing the connection between the first and second circuit patterns prior to the step of separating the common substrate.

The Examiner CANNOT have this issue both ways. He cannot object to the Drawings for failure to show the elements of claim 4 and then disapprove of the requested correction as an introduction of new matter which ALREADY HAS BEEN THE BASIS for the requirement of corrected drawings. By requiring the correction in the First Office Action, the Examiner admits that the testing apparatus is NOT new matter.

Moreover, the process of testing is NOT new matter. See original Specification at page 10, lines 19 – page 11, line 4 and page 12, lines 23-28. Additionally, Applicants understand that since claim 4 is a process claim, normal

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USPTO procedures are not to require a Figure showing the process. See, e.g., MPEP §608.02, where the requirement of a drawing is stated for mechanical and electrical claims but not process claims.

In sum, a new Figure has been submitted, and, alternatively, the above states reasons that the previously proposed correction to Figure 5 should be acceptable.

New Claims

New Claims 22 and 23 were in the original application. New claims 24 and 25 are fully supported, *inter alia*, by the paragraph that begins on page 9, line 23 and ends on page 10, line 3.

Objection to the Specification

In Applicants' Amendment under 35 CFR 1.111, Applicant attempted to amend the paragraph on page 10, beginning on line 16. That Amendment is withdrawn, and a new amendment is submitted wherein the subject paragraph is amended to simply refer to new Figure 11.

Claim Rejections – 35 U.S.C. §102

Claims 1, 5, and 7 were rejected under 35 U.S.C. §102(b) as being anticipated by Wang et al (US 5,419,038). In response, the claims have been amended to make clear that Applicants' invention pertains to circuit boards. Moreover, the step of connecting has been replaced with a step of "fastening pre-formed electrical wires". Wang pertains to thin film depositions on chips coupled with etched removal of substrates and entirely lacks any teaching of circuit boards, of "fastening" steps, or of using pre-formed electrical wires. The electrical connections in Wang are made by depositing thin film strips and the etching away of substrate. Wang thus lacks important elements of the claims as amended, namely, a process step involving "fastening" and the application of this step to "pre-formed wires".

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Additionally, Wang's teachings regarding semiconductor manufacturing are entirely nonanalogous art to the present invention relating to circuit boards.

In sum, the claims have been amended to make clear that the present invention applies to circuit boards that are electrically connected by fastening pre-formed electrically conductive wires and not to the non-analogous art of semiconductor manufacture using deposition and etching techniques. Wang thus neither teaches key elements of the present invention nor is analogous to the present invention.

Claim Rejections – 35 U.S.C. §103

Claims 2-3, 10-11, 14-16, and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang et al (US 5,419,038) in view of Latasiewicz (US 4,316,235). Claim 1 is the only independent claim in the Application, and allowance of Claim 1 as discussed above requires allowance of all other claims in the Application since these depend from Claim 1.

In addition, Latasiewicz fails to cure the failure of Wang to teach the elements of Claim 1 since, as discussed in Applicants' First Amendment under 35 CFR 1.111, Latasiewicz fails to teach the tilting step of claim 1 and is nonanalogous art. Specifically, the problem solved in Latasiewicz relates to moving a portion of a printed wiring board upward in order for luminescent diodes on that board to become visible to a human viewing the outside casing of the device (in this case, a clock). As shown in Latasiewicz and explained at Latasiewicz, column 2, lines 53-60, the invention in Latasiewicz requires that the separated substrates be moved in a parallel, raised fashion relative to each other. In contrast, the subject of the present invention is the art of joining separate printed wiring boards in order to conserve two-dimensional space (typically horizontal foot print) of a circuit board. Tilting of one board relative to another allows more features to be packed into the same footprint of a board. As disclosed in the specification, this tilting is generally accomplished by

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mounting one board perpendicular to the other, which, by definition, is the maximum "tilting" possible. The invention in Latasiewicz teaches away from such tilting since its goal is simply to raise its diode for better viewing. Any orthogonal tilting would actually move the diodes away from the upper viewing window. Latasiewicz, therefore, teaches away from the present invention.

In sum, Latasiewicz not only fails to teach or disclose the tilting element now included in Claim 1, it is nonanalogous art and teaches away from the present invention. Claim 1 is, therefore, allowable over Latasiewicz. All claims that depend from claim 1 are similarly allowable.

Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 5,419,038)/Latasiewicz (US 4,316,235) in view of Degani et al (US 6,370,766). Degani, however, does not cure the defects of Wang nor teaches or discloses the elements of Claim 1, namely, the creation of multiple electrically connected circuit boards from a common substrate, which multiple circuit boards remain electrically connected both before and after separation from the common substrate. No disclosure of tilting the connected boards relative to each other is contained in Degani. As a result, Degani's limited teaching related to testing multiple boards while still in situ on a common board does not supply the elements missing from Latasiewicz. Claim 1, therefore, is allowable over both Latasiewicz and Degani and the combination thereof. Since Claim 1 is allowable, both Claims 1 and 20 are allowable.

Moreover, with respect to claim 20, the external connection for testing taught by Degani is not within the scope of the element of Claim 20 and is irrelevant to Claim 20. Specifically, the external "connection" in Claim 20 is a further limitation upon the "fastening" in the second element of Claim 1. The second element of Claim 1 requires that the inserting be between the first and second circuit patterns, each of which is on the common substrate. Since Degani only involves external

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connecting with external testing equipment, this is clearly not within the meaning of Claim 20 and is irrelevant.

Claims 8-9 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 5,419,038)/Latasiewicz (US 4,316,235) in view of Official Notice. Official Notice, of course, does not teach or disclose the elements of Claim 1, namely, the creation of multiple connected circuit boards from a common substrate, which multiple substrates remain electrically connected both before and after separation from the common substrate. No disclosure of tilting the connected boards relative to each is included within any Official Notice of a method of separating boards. Claim 1, therefore, is allowable over both Latasiewicz and Official Notice of methods of separating boards and the combination thereof. Since Claim 1 is allowable, each of Claims 8-9 and 19 is allowable.

Claim 17 was rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 5,419,038)/Latasiewicz (US 4,316,235) as applied to claim 2-3, 10-11, 14-16, and 18 above, and further in view of Feeney (US 3,780,430). Claim 17 was rejected under 35 U.S.C. 103(a) as being unpatentable over Latasiewicz (US 4,316,235) in view of Feeney (US 3,780,430). In response, Applicant cannot determine which portion of Feeney teaches holding a substrate in proximity to a sidewall of a cabinet that houses the separated substrates.

Regardless, Feeney does not teach or disclose the elements of Claim 1, namely, the creation of multiple connected circuit boards from a common substrate, which multiple substrates remain electrically connected both before and after separation from the common substrate. No disclosure of tilting the connected boards relative to each other is contained in Feeney. As a result, Feeney's limited teaching of a method of manufacturing multiple boards while still in situ on a common board does not supply the elements missing from Latasiewicz. Claim 1, therefore, is allowable over both Latasiewicz and Feeney and the combination thereof. Since Claim 1 is allowable, each of Claims 8-9 and 19 are allowable.

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In sum, Claims 1-5, 7-10 and 14-25 are pending. Each is believed to be in condition for allowance.

In the event the Examiner considers personal contact advantageous to the disposition of this case, the Examiner is hereby authorized to call Applicant's Attorney, Richard Spooner, at Telephone Number (585) 423-5324, Rochester, New York.

Respectfully submitted,

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Application No. 09/09/746,774

Part of #10

VERSION WITH MARKINGS TO SHOW CHANGES MADE:

IN THE SPECIFICATION

Amended paragraph on page 10, beginning at line 16:

Turning now to Figure 7, a perspective view of the process step of Figure 6 is shown. As shown, all of the components of both PWB 4 and PWB 5 can be assembled and completed prior to the separating and/or tilting step. Moreover, complete circuit and functional testing of individual boards PWB 4 and PWB 5 can be completed simultaneously, thereby avoiding inventory and handling expenses and problems. Such testing is exemplified by [testing fixture 60 shown in Figure 5 because] the exemplary process shown in Figure 11. Moreover, because connectors 11-14 are already inserted on single substrate board 2 prior to separation or tilting, then the entire PWB assembly of both boards can be completely circuit and functionally tested prior to separation. This is a major advantage over the prior art since, as discussed above, such combined testing normally cannot be completed until after each board is separately manufactured, inventoried, handled, retrieved, and inserted in a socket fixture. Under the prior art, when the combination of boards fails a test, the correction process must both determine whether the defect occurred in the connecting and fixturing process or whether a defect occurred on one of the boards due to mishandling during handling and assembly. In the process of the present invention, testing need occur only once on both the individual and the connected combination of boards.

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IN THE CLAIMS:

1) (Twice Amended) An improved process for manufacture and assembly of a plurality of adjoined printed wiring boards, comprising:

(a) forming at least a first circuit pattern and a second circuit pattern on a common circuit board substrate;

(b) fastening at least one electrically conductive pre-formed wire to connect[ing] at least the first circuit pattern to the second circuit pattern;

(c) separating the common circuit board substrate into at least a first substrate and a second substrate with the first substrate including the first circuit pattern thereon and the second substrate including the second circuit pattern thereon; and

(d) tilting the first substrate relative to the second substrate while maintaining the connection between the first circuit pattern and the second circuit pattern.

2) (Twice Amended) The process of **claim 1**, further comprising scoring the common circuit board substrate along a dividing line.

4) (Twice Amended) The process of **claim 1**, further comprising testing the connection between the first and second circuit patterns prior to the step of separating the common circuit board substrate into separate substrates.

5) (Amended) The process of **claim 1**, wherein the step of separating occurs after the step of [connecting] fastening.

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7) (Amended) The process of **claim 1**, wherein:

(a) the common circuit board substrate comprises at least a first substrate section and a second substrate section;

(b) the step of forming comprises forming a plurality of circuit patterns on the first substrate section and a plurality of circuit patterns on the second substrate section; and

(c) the step of [connecting] fastening further comprises making a plurality of connections between circuit patterns on the first substrate section and the second substrate section.

8) (Amended) The process of **claim 1**, wherein the step of separating further comprises pressing the common circuit board substrate along a dividing line until it separates into at least the first and second substrates.

9) (Amended) The process of **claim 1**, wherein the step of separating further comprises cutting the common circuit board substrate into a plurality of separate substrates.

Claim 10 was cancelled.

11) (Amended) The process of **claim [10] 1**, wherein the at least one electrically conductive wire comprises a pre-insulated wire.

19) (Amended) The process of **claim 1**, wherein the step of separating further comprises using an edged tool placed in contact with the common circuit board substrate along a dividing line.

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20) (Amended) The process of **claim 3**, wherein the step of [connecting] fastening further comprises [making] connecting at least one electrically [connection that is external] conductive pre-formed wire externally from the holding fixture.

Claims 21-25 are new.

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